High density 3D integration solutions at the wafer scale

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Context

- Leti's enabling technologies for the future of computing
- Focus of this talk:

3D Integration Solutions at the wafer Level
Contents

- Brief history of 3D at Leti
  - Today's investments in success
- The evolution of 2.5D and 3D
  - Leti's position in 2.5D
    - Recent demonstrators, future directions
  - Leti's position in 3D, recent demonstrators
  - Future direction of 3D at Leti
    - High Density Via last and Direct Bonding
    - Monolithic
- Summary
Long history of 3D technology at Leti

Laser drilled TSV, Patented 1988
R. Cuchet et al., 1998.

1995: Vertical 3D Stacking

1999: MCM 3D

CIS program, 2005 – 2008
- Wafer Scale Packaging for CMOS Imaging Sensors

ECTC 2008 D. Henry & Al.

1st Yield > 98%

1st Photograph
Consumer application enabling advanced science!

- **ALICE: A Large Ion Collider Experiment**

  2x 5 Chip Ladder Si Pixel detector
  Ladder = Units of 5 read-out chips mounted on detector

- **Problem description**
  - Low resolution spots between chips
  - Blind spots between ladders

- **Solution**
  - Through Silicon Vias → 3D
    - Buttable tiles and dice
    - Interconnects within-chip, no pads creating blind spots
  - Similar requirements for medical applications

TSV processing of Medipix3 wafers by CEA-LETI: a progress report. T.Tick, M.Campbell TWEEP 2011
Investment in Success

- Fully equipped 3D-300mm line
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Evolution from 2.5D to 3D?

2.5D
- Passive Si Interposer
  - Only wiring and contacts (RDL)
- Can be manufactured in Front End or Back End lines
  - But realistically: FE is too costly!

3D
- Active Si Interposer
  - Si contains active CMOS
  - In other words: a chip
  - Front End manufacturing Only

Break in evolutionary Link
- 2.5D and 3D are evolutionary cousins
- But 2.5D does not necessarily evolve into 3D
- Co-existing technologies
  - But different value and supply chains!

Leti delivering results in both branches

Indonesian crested black macaque, Courtesy BBC
2.5D

Two ways of thinking “silicon interposer”

High Density Interposer

More wires…

Smart Interposer

More than wires…
Si Interposer Demonstrator

- Features
  - Cu TSV, AR10
  - 2 to 4 layers routing, Damascene thick copper, L/W 0.5/0.5 x 1.4μm
  - Temporary bonding
  - Thinning, Stress Monitoring, Warp Management
High density 3D integration solutions at the wafer scale.


**Tomorrow: Smart Interposer**

- **Evolution Continues**

- **RDL Interposer**
  - Multidice
  - TSV
  - Double sided

- **Passives Interposer**
  - Passives in RDL
  - MEMS Clocks
  - 3D capacitors
  - Antennae

- **Photonic Interposer**
  - Photonic converter (CTB)
  - Chip to Chip link

- **Thermal Interposer**
  - Computing
  - Power
  - Lighting
  - Application processor
  - Passive Thermal Enhancer
  - Active cooling

- **Photonic Interposer**
  - Chip to Chip link

**RF Platform for Baseband**
- Data converters
- Lighting
- Application Processor (decoupling capacitance)
- Health: Implantable electronics
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### 3D Partitioning Demo: Digital - Analogue

- **Wireless application**
  - High definition video transmitter, >1GHz
  - Integration technology proven and concept demonstrated
    - TSV + 7 metal layers, 65nm technology
  - Cost evaluation dependant on product complexity and design

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3D Integration of a Wireless product with Design Partitioning

G. Druais et al., 3DIC 2012
Wide I/O Demonstrator

- **Wide I/O**
- **TSV’s**
  - Ø 10 μm, AR 8, Pitch 40 μm, Number 1016
  - Compatible with FD-SOI
- **Chip to Chip Cu Pillars**
  - Ø 20 μm, Height 20 μm, Pitch 40 μm, Number 1016
- **SoC to Substrate Cu Pillars**
  - Ø 55 μm, Height 40 μm, Pitch > 200 μm, Number 933
- **FBGA Package**
  - Size 12x12mm, Ball Pitch 0.4mm, Ball Matrix 29x29, 1.2 mm thickness

WIOMING, G.Kimmich, G.Qualizza 2012-06-28
Next Stage?

- **Current TSV approach is Via Middle**
  - Minimized via dimension → minimized Si surface loss
  - Works well in Si interposers
    - Fits with supply chain
    - Can give competitive advantage
  - Demonstrated for 3D integration
  - Scalability uncertain
    - Optimum node for 3D introduction unclear

- **What if TSV Via Last can produce even smaller vias?**
  - Possible with permanent bonding
  - Won’t work with current 2.5D model
  - Might not work for fabless + foundry model
  - Could work for IDM’s
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High Density TSV’s, functional 65nm MOSFETs

- First TSV’s integrated in 65nm technology
- First experimental evidence of TSV / MOSFET coupling
  ... and in agreement with modeling

Investigation on TSV impact on 65nm CMOS devices and circuits
H. Chaabouni, M. Rousseau, P. Leduc et al., IEDM 2010
Direct bonding - Contact resistance

- Daisy chain measurements with 30k contacts

**Theoretic**  \[ R_{th} = 77\text{mΩ} \]

- Contact resistance is \(~2.5\text{mΩ}, significantly lower than TSV resistance\)
- In accordance with theoretic model

**Experimental**  \[ R_{ex} = 79.5\text{mΩ} \]

- Full characterization of Cu/Cu direct bonding for 3D integration  
  R. Taibi et al. ECTC 2010
- 200°C direct bonding copper interconnects: electrical results and reliability  
  Di Cioccio et al., 3DIC 2012
Reliability Results

- 30,000 Daisy chain
  - 200°C post bonding anneal

- Behaves as one continuous structure without interface between copper lines on the two bonded levels

200°C direct bonding copper interconnects: electrical results and reliability. Di Cioccio et al., 3DIC 2012

Investigation of stress induced voiding and electro-migration phenomena on direct copper bonding interconnects for 3D integration. R. Taibi et al. IEDM 2011
High Density - Via Last

- Scientifically – looks very exciting and promising!
- But many commercial issues to address...
  - Seems limited to IDM’s and Memory applications
    - Intimate co-dependence of design and manufacturing technology
  - Die to Wafer
    - Technically demonstrated
    - Thru-put may always be an issue
      - Very small contacts = very high alignment accuracy required
  - Wafer to Wafer
    - Technically less complicated than DtW
      - Si surface management easier at wafer level
    - Thru-put should be acceptable
    - But it remains nevertheless WtW
      - Design for die size, yield, redundancy, etc.
Monolithic/ Sequential 3D

- Wafers Processed separately
- Stacking and Contacting
- 1 TSV/ Block of 10,000 FETs
- Bottom transistor processing
- Top FET processing
- Contacting
- 1 vertical contact/ FET

Advances, Challenges and Opportunities in 3D CMOS Sequential Integration.
P. Batude et al, IEDM 2011
Nano-scale possibilities

- First demonstration of 3D sequential structure down to $L_G \approx 50\,\text{nm}$
Summary

- Quiet a successful history of 3D integration at Leti
  - Leti TSV’s in consumer production since 2009
  - Fully equipped 3D-300mm line with expert personnel
- Ongoing demonstrators and developments in both 2.5D and 3D
  - Leti has delivered several ‘firsts’
  - Advanced development continues
- Why not join us and share the success?