A 60GHz Reconfigurable Power Amplifier implemented in planar 28nm UTBB FD-SOI CMOS

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Motivation

Challenges with WPAN applications

Linearity/consumption tradeoff

60-GHz transceivers (RF TX part)

Main goal of this work
→ Reduce the consumption at a large power back-off
→ Improve the overall transceiver efficiency
Why CMOS FD-SOI?

Challenges with WPAN applications

Active device: down-scaling

$\text{CMOS down-scaling}$

- $f_T$, $f_{\text{max}}$, Gain
- $P_{\text{out}}$, Linearity

$\text{Indoor applications}$ $\rightarrow$ OFDM modulation

- $f_T$: transition frequency
- $f_{\text{max}}$: maximum frequency of oscillation
- $P_{\text{out}}$: output power
Motivation

Challenges with WPAN applications

Linearity/consumption tradeoff

Can we optimize both linearity and efficiency with CMOS?

→ 28-nm FD-SOI technology and good skills in mmW PA design!!

Achievable?

15.6 dBm, 6%

17.2 dBm, 2%
Motivation

Challenges with WPAN applications

1) HCI (Hot Carrier Injection) degradation

Major failure mechanism for nano-scale CMOS devices

Impact ionization $\rightarrow$ Decrease of $I_D$ vs time

Solution:
- Reduction of $V_{DD}$
  - Reduce electrical field
  - Reduce transistor stress

$\rightarrow$ Low $V_{DD}$, but keep RF performances

Ex: Output transformer with a good isolation can reduce the impact of antenna mismatch on the transistor.

2) High VSWR impact

VSWR related to the antenna mismatch $\rightarrow$ High voltage/current excursion on the drain.

Solution:
- Add a protection to avoid device destruction
Fully depleted (FD) channel due to the buried oxide
\[ \rightarrow \text{back-gate contact } V_{bb} (0V \rightarrow 2V) \text{ to control } V_T \]

10 metal layers + thick alucap :
\[ \rightarrow \text{good passive devices} \]

However :
About **5250** design rules...
28-nm planar UTBB FD-SOI vs Bulk

RF performances

<table>
<thead>
<tr>
<th>150-µm Transistor @60GHz</th>
<th>65nm Bulk</th>
<th>28nm Bulk</th>
<th>28nm FD-SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAG/MSG [dB]</td>
<td>9</td>
<td>11</td>
<td>12.5</td>
</tr>
</tbody>
</table>
Reconfigurable linearized power cell

Segmented bias

Segmented-bias (AB/C)
Operating class controlled by back-gate voltages $V_{B1}$ and $V_{B2}$

@ low-power $\rightarrow$ only class-AB transistors drive current
@ high-power $\rightarrow$ class-C transistors compensate gain compression of main transistors $\rightarrow$ higher linearity and efficiency

Highly efficient compact alternative to Doherty PA

- Dynamic capacitive neutralization with MOS device to track $C_{gd}$
  $\rightarrow$ Better immunity to process and bias variations
NRPC: Neutralized Reconfigurable Power Cell
CL: Coupled Lines → minimize the impact of inductive and resistive return path

Strict density rules
Less than 1dB IL

10 ML stack

minimize the impact of inductive and resistive return path
PA topology

Chip micrograph

TRF1: *Power combiner*
- Power cells
- Power cells

TRF2: *Power splitter*
- 2\(^{nd}\) driver cells
- 1\(^{st}\) driver cells

TRF3: *Interstage matching network*

CL: *Coupled lines*

TRF4: *Input balun*

**Area\textsubscript{CORE}**: 0.16mm\(^2\)**
**Measurement results**

**Small signal**

- **2 main operating modes** configured by body bias only
  - High gain mode with all transistors in class A
  - High linearity mode with the segmented bias technique

- **S-parameters results at** $V_{DD}=1.0V$
  - Two highlighted modes: high gain & high linearity (intermediate modes possible)
  - $>8$ GHz bandwidth
  - Unconditionally stable

![Graph showing S11, S22 dB vs. Frequency (GHz)](image)

**Few variations of reflection coefficients**

- High linearity mode
- High gain mode
Measurement results

Large-signal vs frequency

<table>
<thead>
<tr>
<th>Channel</th>
<th>[GHz]</th>
<th>( P_{\text{SAT}} ) [dBm]</th>
<th>( P_{1\text{dB}} ) [dBm]</th>
<th>( \text{PAE}_{1\text{dB}} ) [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>57.24 - 59.4</td>
<td>19.1 ± 0.1</td>
<td>18.5 ± 0.05</td>
<td>20.9 ± 0.6</td>
</tr>
<tr>
<td>2</td>
<td>59.4 - 61.56</td>
<td>18.9 ± 0.1</td>
<td>18.2 ± 0.25</td>
<td>21.1 ± 0.4</td>
</tr>
<tr>
<td>3</td>
<td>61.56 - 63.72</td>
<td>18.35 ± 0.45</td>
<td>17.7 ± 0.3</td>
<td>19.3 ± 1.4</td>
</tr>
<tr>
<td>4</td>
<td>63.72 - 65.88</td>
<td>17.1 ± 0.8</td>
<td>16.5 ± 0.7</td>
<td>15.0 ± 2.9</td>
</tr>
</tbody>
</table>
Measurement results

60 GHz: Measured gain, PAE and dissipated power vs. P_{out}

<table>
<thead>
<tr>
<th></th>
<th>Gain [dB]</th>
<th>P_{1dB} [dBm]</th>
<th>PAE_{1dB} [%]</th>
<th>P_{DC} [mW]</th>
<th>PAE_{8dB_backoff} [%]</th>
<th>P_{diss@8dB_backoff} [mW]</th>
<th>100 \times P_{1dB}/P_{DC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>High gain mode</td>
<td>35</td>
<td>15</td>
<td>9</td>
<td>331</td>
<td>1.5</td>
<td>331</td>
<td>9.6</td>
</tr>
<tr>
<td>High linearity mode</td>
<td>15.4</td>
<td>18.2</td>
<td>21</td>
<td>74</td>
<td>8</td>
<td>124</td>
<td>89</td>
</tr>
</tbody>
</table>
## Comparison of CMOS PA performances

### Measurement results

<table>
<thead>
<tr>
<th>This work</th>
<th>S. Kulkarni/ISSCC 2014</th>
<th>D. Zhao/JSSC 2013</th>
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<th>E. Kaymaksut/RFIC 2014</th>
<th>A. Siligaris/JSSC 2010</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>28nm UTBB FD-SOI</td>
<td>40nm</td>
<td>40nm</td>
<td>40nm</td>
<td>65nm PD-SOI</td>
</tr>
<tr>
<td><strong>Operating mode</strong></td>
<td>High gain</td>
<td>High linearity</td>
<td>NA</td>
<td>Low/High power</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Supply voltage [V]</strong></td>
<td>1.0</td>
<td>1.0</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
</tr>
<tr>
<td><strong>Freq. [GHz]</strong></td>
<td>61</td>
<td>60</td>
<td>60</td>
<td>63</td>
<td>61</td>
</tr>
<tr>
<td><strong>Gain [dB]</strong></td>
<td>35</td>
<td>15.4</td>
<td>15.1</td>
<td>22.4</td>
<td>16.8 / 17</td>
</tr>
<tr>
<td><strong>P_{SAT} [dBm]</strong></td>
<td>18.9</td>
<td>18.8</td>
<td>16.9</td>
<td>16.4</td>
<td>12.1 / 17</td>
</tr>
<tr>
<td><strong>P_{1dB} [dBm]</strong></td>
<td>15</td>
<td>18.2</td>
<td>16.2</td>
<td>13.9</td>
<td>9.1 / 13.8</td>
</tr>
<tr>
<td><strong>PAE_{max} [%]</strong></td>
<td>17.7</td>
<td>21</td>
<td>21</td>
<td>23</td>
<td>22.2 / 30.3</td>
</tr>
<tr>
<td><strong>PAE_{1dB} [%]</strong></td>
<td>9</td>
<td>21</td>
<td>21</td>
<td>18.9</td>
<td>14.1 / 21.6</td>
</tr>
<tr>
<td><strong>PAE_{8dB_backoff} [%]</strong></td>
<td>1.5</td>
<td>8</td>
<td>7.5</td>
<td>3</td>
<td>- / 4.7</td>
</tr>
<tr>
<td><strong>P_{DC} [mW]</strong></td>
<td>331</td>
<td>74</td>
<td>58</td>
<td>88</td>
<td>56 / 75*</td>
</tr>
<tr>
<td><strong>P_{DC,8dB_backoff} [mW]</strong></td>
<td>332</td>
<td>124</td>
<td>84</td>
<td>94</td>
<td>56 / 78*</td>
</tr>
<tr>
<td><strong>100xP_{1dB}/P_{DC}</strong></td>
<td>9.6</td>
<td>89</td>
<td>72</td>
<td>28</td>
<td>14.5 / 32*</td>
</tr>
<tr>
<td><strong>Active area [mm²]</strong></td>
<td>0.162</td>
<td>0.081</td>
<td>0.074</td>
<td>0.33</td>
<td>0.1</td>
</tr>
<tr>
<td><strong>ITRS FOM [W.GHz²]</strong></td>
<td>161,671</td>
<td>1,988</td>
<td>1,198</td>
<td>6,925</td>
<td>641 / 2,832</td>
</tr>
</tbody>
</table>

### Notes

- High linearity mode → reduce the consumption → improve PAE @CP1
- no compromise on the linearity

ITRS FOM = \( P_{SAT} \cdot PAE_{max} \cdot \text{Gain} \cdot \text{Freq}^2 \)

* with pads  
# estimated
OUTLINE

- Motivation
- 28-nm planar UTBB FD-SOI vs BULK
- Reconfigurable linearized power cell
- PAtopology
- Measurement results
- Reliability discussion
- Conclusion
Max performances at 59GHz @ $V_{DD} = 1.1V$ :
\[ P_{SAT} = 20.2\text{dBm},\ P_{1dB} = 19.5\text{dBm},\ PAE_{1dB} = 22.3\% \]
Low variation from 0.7V to 1.1V (max permitted) \( \Rightarrow \approx 4\text{dBm} \text{ Psat} \) and CP1, 2% PAE
\( \Rightarrow \) can address complex modulation with large back-off \( \Rightarrow \) reduced $V_{DD}$ \( \Rightarrow \) reduced consumption

The circuit is perfectly functional @$V_{DD} = 0.7V$
Reliability discussion

Drain voltage excursion with a high VSWR @ P_{1dB} (simulation)

In practical use, the VSWR is limited at 6 (metal plane placed at 2mm in front of the antenna) → Drain voltage < 2V

The PA is protected thanks to the transformer isolation.
## Reliability discussion

Comparison of CMOS PA performances

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<th>A. Siligaris JSSC 2010</th>
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<th>S. Kulkarni ISSCC 2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech. [nm]</td>
<td>28 (FD-SOI)</td>
<td>65</td>
<td>65(SOI)</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>$V_{DD}$ [V]</td>
<td>0.8</td>
<td>1.0</td>
<td>1.8</td>
<td>1.0</td>
<td>0.9</td>
</tr>
<tr>
<td>Topology</td>
<td>CS</td>
<td>CS</td>
<td>CAS</td>
<td>CS</td>
<td>CS</td>
</tr>
<tr>
<td>$P_{1\text{dB}}$ [dBm]</td>
<td>16.2</td>
<td>12.5</td>
<td>12.7</td>
<td>13.8</td>
<td>13.9</td>
</tr>
<tr>
<td>PAE$_{1\text{dB}}$ [%]</td>
<td>21</td>
<td>-</td>
<td>22.6</td>
<td>21.6</td>
<td>18.9</td>
</tr>
<tr>
<td>PAE$_{8\text{dB, backoff}}$ [%]</td>
<td>7.5</td>
<td>-</td>
<td>2.7</td>
<td>4.7</td>
<td>3</td>
</tr>
<tr>
<td>$P_{DC}$ [mW]</td>
<td>58</td>
<td>600</td>
<td>77.4</td>
<td>75</td>
<td>88</td>
</tr>
<tr>
<td>$100 \times P_{1\text{dB}}/P_{DC}$</td>
<td>72</td>
<td>3</td>
<td>24</td>
<td>31</td>
<td>28</td>
</tr>
</tbody>
</table>
Conclusion

RADAR chart → Global performances of CMOS PA

Previous references
- Zhao, *JSSC* 2013
- Silgaris, *JSSC* 2010
- Kulkarni, *ISSCC* 2014
- Kaymaksut, *RFIC* 2014

This work
(high linearity mode)

*Best linearity/consumption tradeoff!*
Conclusion

60 GHz 28nm FS SOI Power Amplifier

- Fully WiGiG compliant (linearity and frequency range)

- Reconfigurable power cells:
  - Continuous tuning thanks to body bias with 2 extreme modes:
    - High gain mode: *Highest ITRS FOM*
    - High linearity mode: *Break the linearity/consumption tradeoff*
  - High efficiency @ large output power back-off
  - Optimization of the transmitter line-up depending on complex modulation scheme and output power

- Reliable and operational @\(V_{DD} = 0.8V\)
Thank you for your attention!