



**PRESS RELEASE**

## **CEA-Leti Makes a R&D 20nm Fully Depleted SOI Process available through CMP**

**Grenoble, FRANCE, and Tokyo, JAPAN, October 1<sup>st</sup>, 2010, CEA-Leti and CMP (Circuits Multi Projets<sup>®</sup>)** announced during the FDSOI Workshop at Tokyo University the launch of an Exploratory MPW (Multi Project Wafers) initiative based on FDSOI (Fully Depleted SOI) 20nm process, opening the access of its 300mm infrastructure to the design community. This MPW offer is partly supported by EUROSOI+ network that gathers the main European academic partners on SOI.

*"Leti has pioneered the SOI technology for years, leading track records in the most advanced research in FDSOI, assessing its key advantages for low power high performance applications with several industrial customers,"* said Laurent Malier, CEO of CEA-Leti. *"It is time now to enlarge the diffusion of the FDSOI technology enabling test cases on 20nm process and beyond. This hit will change the game, breaking the wall of technology to give an open access to the R&D international design community and a unique opportunity to touch silicon with innovative designs."*

*"CMP is very proud to offer such a very advanced process to the community. Such a process will allow researchers and engineers to experiment with the benefits of SOI on an advanced technology node,"* said Bernard Courtois, head of CMP.

CEA-Leti has been involved with FDSOI R&D for a number of years and has developed internally both an advanced High-K/Metal Gate FDSOI process and a number of specific design and simulation tools based on industry-standard design-flow packages. FDSOI technology presents key advantages over conventional bulk technology for future nodes. The electrostatic integrity of the transistors is ensured by the thinness of the body without the need for extra litho steps, like in the case of FinFETs, or of channel doping. The consequence is a planar technology that exhibits at the same time excellent short channel behavior and significant improvement of the variability as shown in a number of recent papers.

The basis of the technology offer will be the following:

- CMOS transistors with an undoped channel and a silicon film thickness of 6nm
- High-k / Metal Gate stack
- Single threshold voltage ( $V_{th}$ ) n- and pMOSFET with balanced  $V_{th}$  of  $\pm 0.4V$
- Associated Design Kit, including SPICE model (Verilog-A language), model cards extracted from silicon data, p-cells, DRC, LVS, schematic, parasitics
- Design Kit documentation

The first run is scheduled to be launched in September 2011. All details will be available on the CMP website.

### **About CEA-Leti**

CEA is a French research and technology public organisation, with activities in four main areas: energy, information technologies, healthcare technologies and defence and security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. CEA-Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and microsystems (MEMS) are at the core of its activities. As a major player in MINATEC campus, CEA-Leti operates 8,000-m<sup>2</sup> state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards. With 1,200 employees, CEA-Leti trains more than 150 Ph.D. students and hosts 200 assignees from partner companies. Strongly committed to the creation of value for the industry, CEA-Leti puts a strong emphasis on intellectual property and owns more than 1,500 patent families.

For more information about Leti, please visit [www.leti.fr](http://www.leti.fr).

### **About CMP**

CMP is a broker in ICs and MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial Companies. Advanced industrial technologies are available in CMOS, BiCmos, SiGe BiCMOS and MEMS etc. CMP distributes and supports several CAD software tools for both Industrial Companies and Universities. Since 1981, more than 1000 institutions from 70 countries have been served, more than 6000 projects have been prototyped through 700 runs, and 56 different technologies have been interfaced.

For more information, visit: <http://cmp.imag.fr>

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